Numerous different implementations for H.264/AVC variable block size motion estimation have been proposed in the recent years to make this computationally challenging task more feasible for mobile devices with video encoding support. The variable block size motion estimation problem defined by the standard is complex and multidimensional, offering a wide variety of possibilities for efficient implementation. One of the most popular implementation architectures are systolic arrays.

In this paper we look at the full-search variable block size motion estimation problem on 1D systolic arrays from a high level by modeling the system with a software tool that enables design space exploration and cycle-accurate simulation. Our design space exploration tool has provided many interesting insights to the VBSME problem that give directions for making efficient designs.