## Arithmetic Optimization for Custom Instruction Set Synthesis

### Motivating Example

Instruction set extensions (ISEs) accelerate ASIPs.

**Apply arithmetic optimizations to the ISEs to form networks of full-adders.**

**Our Goal:** Optimize the networks for delay.

### Prior Work: Three Greedy Algorithm (TGA)

- Requires a-priori knowledge that the function computed by the network is a multi-input adder.
- Always synthesizes a delay-optimal compressor tree.

### Our Approach

- Requires no a-priori knowledge of the function computed by the network.
- A compressor tree is **not** delay-optimal when input bit arrival times are **highly skewed**.
- Synthesize a delay-optimal full adder network.
- Unlike the TGA, the network synthesized by our approach may contain:
  - Internal carry-propagate adders.
  - Multiple distinct compressor trees.

### All Input Bits Arrive at the Same Time

**Input Bit Arrival Times**

- Naïve Solution (Sub-optimal)

### Input Bit Arrival Times are Skewed

**d >> Delay(FA)**

- TGA Solution (Sub-optimal)

### Swap Signals to Reduce Delay

### Multiple Compressor Trees may be Better than One

**Naïve Solution**
- Delay = 1.65ns
- Area = 18495μm²

**TGA Solution**
- Delay = 1.64ns
- Area = 17876μm²

**Our Solution**
- Delay = 1.48ns
- Area = 17553μm²

### Results

**Normalized Delay**

**Benchmarks**