Interconnect Optimization for High-Level Synthesis of SSA-Form Programs

Register Allocation in Synthesis
- Minimum register allocation is polynomial for SSA Form applications
- Interference graph is chordal
- Optimizing interconnect/multiplexers during register assignment is NP-Complete

**Contribution:** Heuristics to attack the harder problem
- Greedy – Extension of Chordal Coloring
- Simulated Annealing

**Objective**
\[ y \leftarrow \varphi(\ldots, x, \ldots) \]
- \( \text{reg}(x) \neq \text{reg}(y) \) \rightarrow \text{wire from \text{reg}(x) to \text{reg}(y)}
- \( \text{reg}(x) = \text{reg}(y) \) \rightarrow \text{no wire needed}
- Multiplexer on each register input
- **Goal:** Minimize wires/multiplexer sizes

**Color Assignment**
- Interference Edge
- \( \varphi \)-Edge: \( y \leftarrow \varphi(\ldots x, \ldots) \)

**FPGA Area**

<table>
<thead>
<tr>
<th>Method</th>
<th>LUTs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chordal Coloring</td>
<td></td>
</tr>
<tr>
<td>Greedy</td>
<td></td>
</tr>
<tr>
<td>Simulated Annealing</td>
<td></td>
</tr>
</tbody>
</table>